JVSTB
Journal of Vacuum Science & Technology B

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Citation: Journal of Vacuum Science & Technology B **32**, 06FI04 (2014); doi: 10.1116/1.4901420
View online: http://dx.doi.org/10.1116/1.4901420
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/32/6?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Fabrication of silicon nanostructures with large taper angle by reactive ion etching

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(Received 29 July 2014; accepted 30 October 2014; published 12 November 2014)

Micro- and nanostructures with a tapered sidewall profile are important for antireflection and light trapping applications in solar cell, light emitting diode, and photodetector/imager. Here, the authors will show two etching processes that offer a large taper angle. The first process involved a maskless etching of pre-etched silicon structures having a vertical profile, using a recipe that would give a vertical profile when masked. The authors obtained a moderate taper angle of 14° using CF_4/O_2 etching gas. The second process involved a one-step etching step with Cr as mask using a recipe that was drastically modified from a nonswitching pseudo-Bosch process that gives a vertical profile. The gas flow ratio of C_4F_8/SF_6 was greatly increased from 38/22 to 59/1 to result in a taper angle of 22°. Further reduction of the RF bias power led to an unprecedented large taper angle of 39° (at the cost of greatly reduced etching rate), which is even higher than the angle obtained by anisotropic wet etching of silicon. © *2014 American Vacuum Society*.
[http://dx.doi.org/10.1116/1.4901420]

I. INTRODUCTION

Dry etching is the preferred pattern transfer method since it offers a tunability of the etching profile, whereas the profile is usually not tunable for wet etching, with a curved profile resulted from an isotropic etching being the most typical. For majority applications, a completely anisotropic etching is desired since the resulted vertical profile retains the critical dimension of the mask and enables the etching of high aspect ratio structures.[1,2] However, for some applications, a tapered profile is beneficial. For instance, a tapered profile in combination with a back-side reflector can be employed for light trapping to enhance the energy conversion efficiency of solar cell, or to allow the use of a thinner absorber material while maintaining an acceptable energy efficiency.[3] Here, the light trapping is based on multireflection that greatly increases the optical light path within the solar cell system, and the feature size of the light trapping structure is in the range of microns for which ray optics can be applied. For subwavelength nanoscale tapered structures, they can be employed for antireflection purpose in light emitting diodes, photo-detectors, and solar cells.[4] Here the tapered subwavelength structures lead to an effective index gradient at the interface between optical media having different indices of refraction, which drastically reduces surface Fresnel reflection over a broad spectral range and a wide field of view. Other applications of tapered structure include diffuser or nozzle for microfluidic devices, and via for through-silicon interconnection that is a critical and enabling technology for 3D stacking of electronic and electromechanical systems.[5]

Various techniques have been developed to achieve a tapered etching profile. For wet chemical etching, KOH or tetramethylammonium hydroxide (TMAH) is commonly used to anisotropically etch crystalline silicon; but this process gives only one fixed taper angle of 35.3° when etching (100) silicon.[6] For dry etching, small taper angle ($<10°$) can be readily achieved by slightly modifying the recipe that gives a vertical profile.[7] However, taper angle of $>20°$ is more challenging to achieve and thus rarely reported in the literature. Obviously one can achieve a large taper angle, using a completely anisotropic etching recipe, if the mask itself has a tapered profile. Such an etching mask can be obtained either by grayscale lithography if the feature size is large ($>1\,\mu$m),[8] or by a liftoff process, which results in tapered metal mask structures due to lateral deposition that gradually closes the opening of the resist template.[4] Very large ($>10\,\mu$m) tapered structure can also be attained using the RIE lag effect that refers to the decrease of etching rate (thus pattern depth) as the hole or trench shrinks, followed by an isotropic etching step to remove the thin walls between the holes or trenches.[9] Another method is to utilize the lateral erosion of the etching mask that results in a gradual shrinking of the mask structure.[10] However, this method inherently necessitates a small etching selectivity between the mask and the material to etch, and thus a thick mask would be needed to etch a tall structure in the target layer. Finally, for dry etching with gas switching, one can obtain tapered profile by adding a SF_6 etching step after a certain number of the standard Bosch process cycles; but this process results in a scallop sidewall.[11]

In this paper, we will show two (nonswitching) dry silicon etching processes that give a large taper angle. The first

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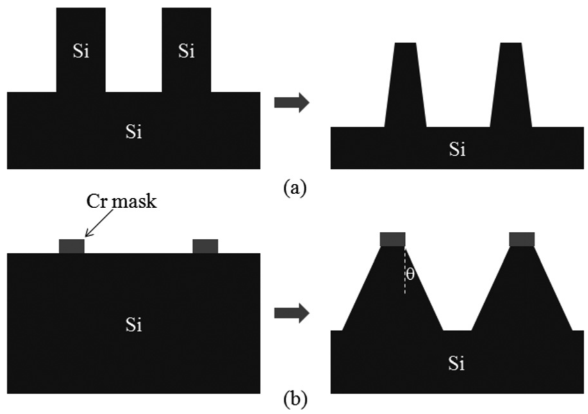

FIG. 1. Two dry etching processes for the fabrication of tapered structure. (a) Maskless etching of pre-etched silicon structures having a vertical profile, using a recipe that would give a vertical profile when masked. (b) Masked etching with a recipe that was drastically modified from a nonswitching pseudo-Bosch recipe shown in Table I.

process started with a vertical profile, and converted it into a tapered one after an additional maskless etching step that eroded the silicon structure laterally while etching along the vertical direction. The second process is based on a drastic modification of the nonswitching pseudo-Bosch recipe to greatly enhance the inhibitor formation, which resulted in a taper angle as large as 39° at the cost of reduced etching rate. We conclude that the second method is more controllable and tunable, and is thus more suitable for light trapping or antireflection structure fabrication.

II. EXPERIMENT

To fabricate the Cr hard etching mask, we carried out electron beam lithography using ZEP-520A resist and a Raith 150^{TWO} system at 20 keV energy and 0.2 nA beam current. Afterward, 40 nm Cr was deposited by electron beam evaporation and lifted off in anisole.

For the first process [Fig. 1(a)], with the patterned Cr as a hard mask, we first etched the silicon for 1000 nm deep using a recipe that gives a vertical profile: Trion Phantom II RIE system, CF_4 20 sccm, O_2 3 sccm, RF power 100 W, ICP power 0 W, and pressure 20 mTorr. The etching rate was 80 nm/min. Then, we removed the Cr film by dipping the sample for 5 min in an etchant consisting of 20% ceric ammonium nitrate, 5% nitric acid, and 75% water. Finally, we carried out mask-less silicon etching using the same recipe for 5 min that etched 400 nm silicon. This second etching gave significant lateral etching because it was not masked.

For the second process [Fig. 1(b)], starting from the standard Bosch process, several research groups have developed silicon etching recipes that give vertical profile and are capable of etching ultrahigh aspect ratio nanostructures.[12–15] Those recipes have either no or very small sidewall scallop depending on whether it is a nonswitching process or a switching one yet with very short cycle time. For our work, we chose the recipe reported in Ref. 14 and shown in Table I as the starting point. This recipe is a nonswitching deep silicon etching process using SF_6 and C_4F_8 gas for, respectively, etching and passivation, and it was previously employed to etch high aspect ratio silicon structures of 100 nm width and 3.5 μm height (aspect ratio 1:35).[13] One can generally obtain tapered profile by promoting inhibitor (here fluorocarbon polymer) formation and decreasing its removal rate, which can be realized by increasing the ratio of C_4F_8/SF_6, reducing the RF bias power or substrate temperature, and/or increasing the gas pressure. In the experiment, we systematically reduced the C_4F_8/SF_6 gas flow ratio from the starting point of 38/22 to 59/1 (total gas flow was fixed at 60 sccm) and the RF bias power from 20 to 10 W, while keeping the other parameters fixed.

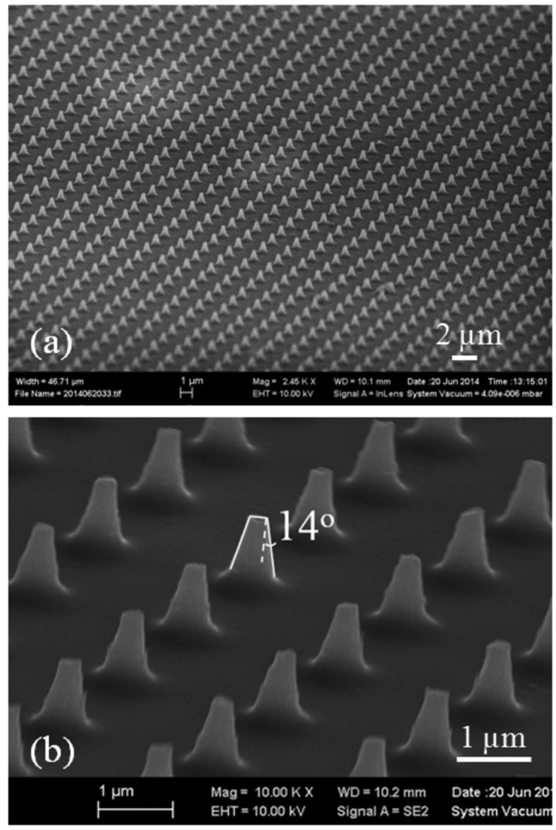

FIG. 2. Low (a) and high (b) magnification SEM images of silicon pillar array with tapered profile fabricated by mask-less etching of silicon pillars having vertical profile. The pillar height remained 1000 nm after etching, and the resulted taper angle was 14°. The pillar diameter at the top shank from 800 to 240 nm due to lateral etching.

III. RESULTS AND DISCUSSION

Figure 2 shows the SEM image of silicon nanostructures with tapered profile fabricated using the first process

TABLE I. Nonswitching pseudo-Bosch recipe that gives a perfect vertical profile (Ref. 13) using an Oxford ICP-RIE system (ICP 380).

C_4F_8 (sccm)	SF_6 (sccm)	RF power (W)	ICP power (W)	Pressure (mTorr)	Temperature (°C)	Si etch rate (nm/min)
38	22	20	1200	10	20	400

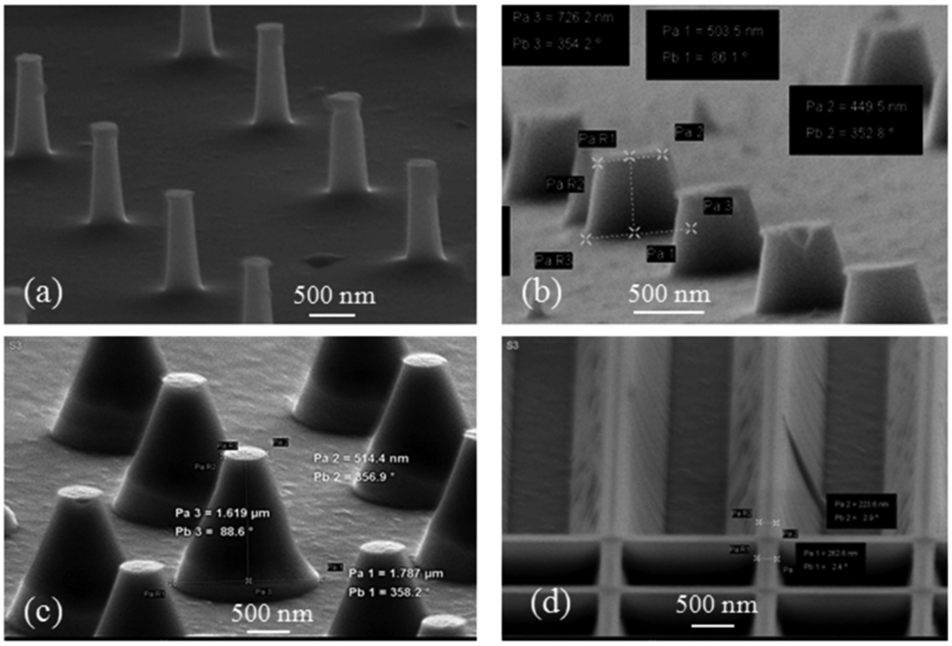

FIG. 3. SEM images of silicon structures etched with different C_4F_8/SF_6 ratios (the other parameters were the same as shown in Table I). The ratios and taper angles are: (a) 50/10, 4.7°; (b) 55/5, 15°; (c) and (d) 59/1, 22°. The sidewall taper angle is calculated based on the measured diameters and heights, and the Cr mask was not removed.

mentioned above. The pillar height of 1000 nm was unchanged after 400 nm maskless etching. The pillar diameter at the top shrank from 800 to 240 nm, corresponding to a radius shrinkage of 280 nm and lateral/vertical etching ratio of 280/400 = 0.7. The resulted taper angle [marked as θ in Fig. 1(b)] was a moderate value of 14° (the angle was calculated based on the measured diameters and height). We have varied the etching parameters, particularly the pressure, but were not able to achieve a higher taper angle. In addition, there was a large slop at the pillar bottom where the pillar meets the bulk substrate, and the pillar top was found slightly rough after the mask-less etching. We conclude that, though this process can result in a tapered profile, it has a limited tunability of the taper angle.

For the second process based on the nonswitching pseudo-Bosch process, we first fixed all the parameters as shown in Table I but decreasing gradually and systematically the gas flow ratio of SF_6/C_4F_8 while keeping the total gas flow fixed at 60 sccm. Rather unexpected, as shown in Figs. 3 and 4, the sidewall taper angle was found not so sensitive to the gas flow ratio. Therefore, we had to decrease the ratio drastically, to the tool limit of 1/59, which led to a large taper angle of 22°. At this gas flow ratio, the etching rate was greatly reduced from 400 nm/min for the baseline recipe with $SF_6/C_4F_8 = 22/38$ to 33 nm/min, which is expected owing to the simultaneous enhanced passivation by C_4F_8 and reduced etching by SF_6. It is also noted that there was no noticeable undercut etching below the Cr mask. As it was not possible to further reduce the gas flow ratio, we reduced the RF bias power from 20 to 10 W, which led to a very impressive taper angle of 39° (Fig. 5), even higher than the angle achieved by KOH anisotropic wet etching of silicon (35.3°). The etching rate was further decreased to 15 nm/min. Due to the excess

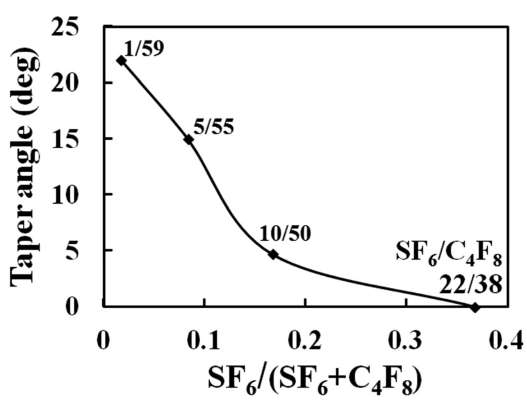

FIG. 4. Dependence of taper angle, as measured in Fig. 4, on the ratio of SF_6 flow and total gas flow (fixed at 60 sccm). The flow ratio of SF_6/C_4F_8 is also indicated.

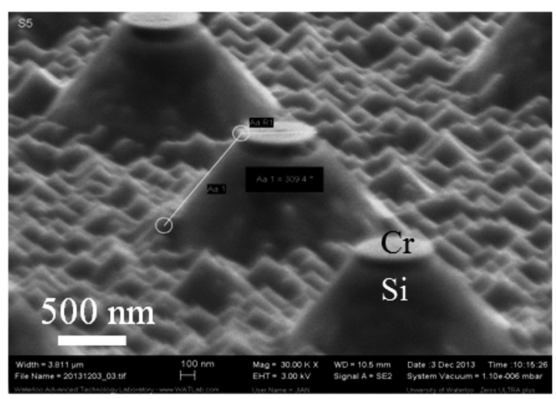

FIG. 5. SEM image of silicon structures etched with RF bias power 10 W and gas flow ratio $C_4F_8/SF_6 = 59/1$ for 50 min (the other parameters were the same as shown in Table I). The sidewall taper angle was calculated as 39°. Cr mask was not removed.

inhibitor fluorocarbon polymer formation, the etched surface was rough, yet this could be advantageous for light trapping application. Further reducing the RF bias power to 5 W led to negligible etching of silicon (not shown).

IV. SUMMARY AND CONCLUSIONS

We demonstrated two different etching processes that can be used to fabricate silicon nanostructures with a large taper angle. The first process involved a mask-less etching of pre-etched silicon structures having a vertical profile, using a recipe that would give a vertical profile when masked. A tapered profile was resulted due to lateral etching, and we obtained a moderate taper angle of 14° using CF_4/O_2 etching gas. The second process involved a one-step etching step with Cr as mask using a recipe that was drastically modified from a nonswitching pseudo-Bosch process that gives a vertical profile. To promote a tapered sidewall profile, the gas flow ratio of C_4F_8/SF_6 was greatly increased from 38/22 to 59/1, which resulted in a taper angle of 22°. Further reduction of the RF bias power led to a very impressive taper angle of 39° that is even higher than the angle obtained by anisotropic wet etching of silicon using KOH or TMAH. However, as expected, the large taper angle was accompanied by a drastically reduced etching rate. The fabricated tapered structures may find applications for antireflection and light trapping for solar cell, light emitting diode, and photodetector/imager.

ACKNOWLEDGMENTS

This work was carried out using the nanofabrication facility at Quantum NanoFab and Giga-to-Nanoelectronics Laboratory funded by the Canada Foundation for Innovation, the Ontario Ministry of Research and Innovation, and Industry Canada. C.C. acknowledges The Ministry of Turkish National Education for financially supporting his study. A.A. acknowledges the financial support from Saudi Arabian Cultural Bureau in Canada as well as the Saudi Ministry of Higher Education (MOHE).

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